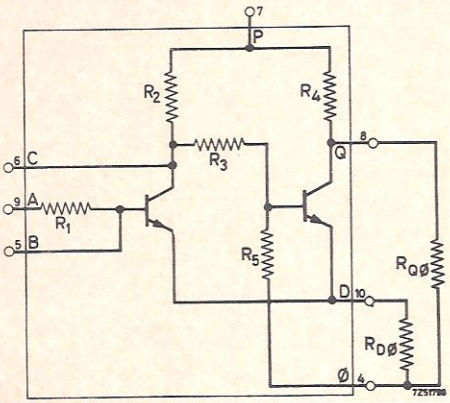
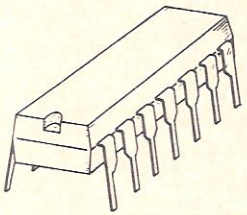
LEVEL DETECTOR

development sample data





Red binder Integrated circuits

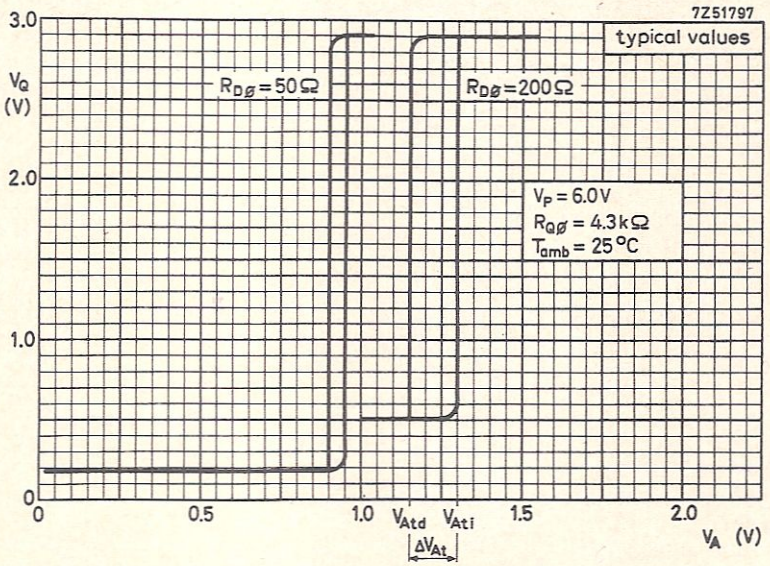
QUICK REFERENCE DATA

Supply voltage		V_P	6.0 ± 5%	V
Operating ambient temperature range		T_{amb}	0 to 75	°C
Clock rate (full temperature range)		f_c	0 to 1	MHz
Input hysteresis voltage (Schmitt trigger operation)	$R_{DØ}$ = 10 Ω	ΔV_{At}	typ. 10	mV
	$R_{DØ}$ = 200 Ω	ΔV_{At}	typ. 150	mV
Available fan-out to FCH gates; T_{amb} = 25 °C		N_a	min. 3	
Power consumption, 50% duty cycle; T_{amb} = 25 °C		P_{av}	max. 19	mW
Package				D1 (Dual in-line)

The FCL101 is a non-inverting bistable circuit which changes states abruptly when the input signal exceeds specific d.c. triggering levels. It is recommended for discrimination, restoration and shifting of signal levels and for squaring of non-rectangular waveforms. The triggering (tripping) levels for increasing and decreasing input voltages are determined externally, either by a resistor ($R_{DØ}$: Schmitt trigger operation) or, for extremely low hysteresis, by a zener diode. The FCL101 is compatible with the other circuits of the FC family.

These data, based on the specifications and measured performance of development samples, afford a preliminary indication of the characteristics to be expected of the described product. Distribution of development samples implies no guarantee as to the subsequent availability of the product

VOLTAGE TRANSFER CURVES



Letter symbols:

$R_{QØ}$ = external resistor between Q and Ø.

V_{QD} = voltage at Q with respect to D.

V_Q = short for $V_{QØ}$ = voltage at Q with respect to Ø, the common reference and supply return terminal.

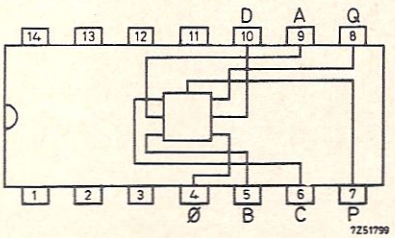
V

V_{Ati} = tripping level for increasing input voltage V_A (short for $V_{AØ}$).

V_{Atd} = tripping level for decreasing input voltage V_A.

$\Delta V_{At} = V_{Ati} - V_{Atd}$ = input hysteresis voltage.

TERMINAL CONNECTIONS (top view)



CHARACTERISTICS

Terminals B and C floating

	Electrical conditions: output Q	Electrical conditions: $R_{D\emptyset}$ (Ω)	Electrical conditions: supply P(V)		T_{amb} (°C): 0	T_{amb} (°C): 25	T_{amb} (°C): 75	
STATIC DATA								
Tripping levels		10		typ.		0.85		V
				max.	1.20	1.20	1.20	V
- input voltage increasing	$R_{Q\emptyset}$ = 4300 Ω	50	6.0	V_{Ati} typ.		0.95		V
		100		typ.		1.10		V
		200		typ.		1.30		V
		10		typ.		0.84		V
				max.	0.50	0.55	0.45	V
- input voltage decreasing	$R_{Q\emptyset}$ = 4300 Ω	50	6.0	V_{Atd} typ.		0.90		V
		100		typ.		1.00		V
		200		typ.		1.15		V
Input hysteresis voltage	$R_{Q\emptyset}$ = 4300 Ω	10	6.0	ΔV_{At} typ.		10		mV
		50		typ.		50		mV
		100		typ.		100		mV
		200		typ.		150		mV
Output voltage								
- output LOW	I_{QL}	10 to 200	5.7	V_{QDL} max.	0.4	0.4	0.4	V
- output HIGH	$R_{Q\emptyset}$ = 4300 Ω	10 to 200	5.7	V_{QDH} min.	2.5	2.5	2.5	V
Output current								
- output LOW $V_{QD} \leq 0.4$ V	-	-	-	I_{QL}	4.0	5.7	3.6	mA
DYNAMIC DATA								
Max. clock rate (operating frequency)	-	10 to 200	6.0	f_c min.	1	1	1	MHz
				typ.		5		MHz
SUPPLY								
Supply current								
- output LOW	$I_Q \leq I_{QL}$	10 to 200	6.3	I_{PL} max.	4.0	3.5	3.2	mA
- output HIGH	$-I_Q \leq 100\ \mu A$	10 to 200	6.3	I_{PH} max.	2.9	2.6	2.4	mA
Power supply consumption 50% duty cycle	as for I_{PL}, I_{PH}	10 to 200	6.3	P_{av} max.	22	19	18	mW

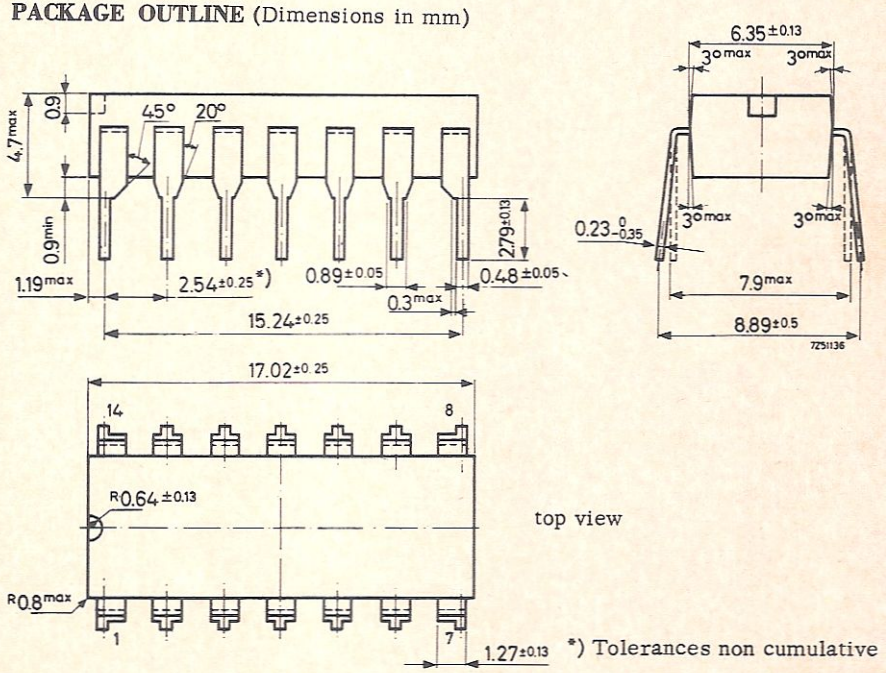
ADDITIONAL SYSTEM DESIGN DATA

	supply P (V)		T_{amb} (°C)			
			0	25	75	
Fan-out to gates FCH101...211	5.7 to 6.3	N_a min.	2	3	2	kΩ
Circuit resistance values	–	R_1 typ.		1.0		kΩ
	–	R_2 typ.		3.3		kΩ
	–	R_3 typ.		1.0		kΩ
	–	R_4 typ.		4.7		kΩ
	–	R_5 typ.		13		kΩ

RATINGS (Limiting values) [1]

Supply voltage	V_P	max. 10	V
Output voltage	V_Q	0 to 8	V
Input voltage	V_A	−6 to +8	V
Storage temperature	T_{stg}	−35 to +125	°C
Operating ambient temperature	T_{amb}	0 to 75	°C

PACKAGE OUTLINE (Dimensions in mm)



*) Tolerances non cumulative

1) Limiting values according to the Absolute Maximum System as defined in IEC publication 134.